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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,672	10/16/2003	Bruce B. Doris	FIS920030247US1	2671

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EXAMINER	
ISAAC, STANETTA D	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 11/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,672	DORIS ET AL.	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 4-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 4-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the amendment filed on 7/28/04. Currently, newly amended claims 1, 4-18, are now pending. Claims 2 and 3 have been canceled.

Specification

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

Claim 1 is objected to because of the following informalities: On, line 5, the word "traverse" should read "transverse". Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 4, and 12-14, are rejected under 35 U.S.C. 102(b) as being anticipated by Jin et al. US Patent 5,940,716.

Jin discloses the semiconductor structure as claimed. See figures 1-24, and corresponding text, pertaining to claim 1, where Jin teaches a semiconductor structure formed on

a substrate, comprising a shallow trench isolation having at least one overhang **108C** selectively configured to prevent oxidation induced stress in a determined portion of the substrate, wherein one of the at least one overhang is selectively configured to prevent oxidation induced stress in a direction parallel to or transverse to a direction of a current flow (figure 14; col. 2, lines 10-22; col. 4, lines 10-13; col. 5, lines 10-21, ***Note***: it is inherent that a direction parallel to or transverse to direction of a current flow is included based on the teachings of Jin, to eliminate the conventionally known problem of stress that can promote the generation of leakage currents that will deteriorate the characteristics of the devices formed in an adjacent active region. In addition, the photoresist or hardmask, taught by Admitted Prior Art, on page 7, paragraph [0028], are well known in the art of semiconductor fabrication. Therefore, it is inherent that one of ordinary skill can control where the overhangs are selectively configured to prevent oxidation induced stress in a direction parallel to or transverse to a direction of a current flow based on the selective application of the photoresist or hardmask used to form the overhangs).

Pertaining to claim 4, Jin teaches the semiconductor structure, wherein: the determined portion of the substrate is a Si-SiO_2 interface adjacent to the shallow trench isolation; and the at least one overhang extends beyond the Si-SiO_2 interface, preventing oxidation at or near the Si-SiO_2 interface (figure 14).

Pertaining to claim 12, Jin teaches the semiconductor structure of claim 1, wherein the overhang includes a T-shaped structure (figure 14).

Pertaining to claim 13, Jin teaches the semiconductor structure of claim 12, wherein the determined portion of the substrate is a Si-SiO_2 interface adjacent to the shallow trench isolation (figure 14).

Pertaining to claim 14, Jin teaches the semiconductor structure of claim 13, wherein the overhang includes a horizontal portion that extends beyond the Si-SiO_2 interface by about 0.01 microns to 0.5 microns (figure 14; col. 4, lines 38-52).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5-11 and 15-18, are rejected under 35 U.S.C. 103(a) as being unpatentable over Jin et al. US Patent 5,940,716 in view of Trivedi US Patent 6,583,060.

Jin discloses the semiconductor structure substantially as claimed. See the preceding claims 1, 4, and 12-14, rejected under 35 U.S.C. 102(b).

However, Jin fails to show, pertaining to claims 5-11 and 15-18, the semiconductor structure comprising: a first device (n-channel field effect transistor) having a source and drain with a direction of current flow (from the source to the drain) for the first device, and a second device (p-channel field effect transistor) having a source and drain with a direction of current flow (from the source to the drain) for the second device. In addition, Jin fails to show, pertaining to claim 16, the semiconductor structure, wherein the distance from the gate of the p-channel field effect transistor to the fourth shallow trench isolation side is less than or equal to about 5.0 microns. Also, Jin fails to show, pertaining to claim 17, the semiconductor structure, wherein the distance from the gate of the n-channel field effect transistor to the first shallow

trench isolation side is less than or equal to about 5.0 mircrons. Finally, Jin fails to show, pertaining to claim 18, the semiconductor structure, wherein the distance from the gate of the n-channel field effect transistor to the second shallow trench isolation side is less than or equal to about 5.0 microns.

Trivedi teaches, in figures 1-15, and corresponding text, a CMOS semiconductor structure having p-channel and n-channel field effect transistors, that includes the use of a dual depth trench isolation structure formed between isolation structures (figure 12; col. 1, lines 5-36).

It would have been obvious to one of ordinary skill in the art to incorporate, a semiconductor structure comprising: a first device (n-channel field effect transistor) having a source and drain with a direction of current flow (from the source to the drain) for the first device, and a second device (p-channel field effect transistor) having a source and drain with a direction of current flow (from the source to the drain) for the second device, in the method of Jin, pertaining to claims 5-11 and 15-18, according to the teachings of Trivedi, with the motivation that, the CMOS semiconductor structure having p-channel and n-channel field effect transistors, taught in Trivedi, includes trench isolations regions used for isolation between neighboring FET devices, for the purpose of reducing the formation of undesirable leakage paths between opposite biased regions.

Response to Arguments

Applicant's arguments with respect to claims 1-18 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on 571-272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stanetta Isaac
Patent Examiner
October 29, 2004

John F. Niebling
Supervisory Patent Examiner
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